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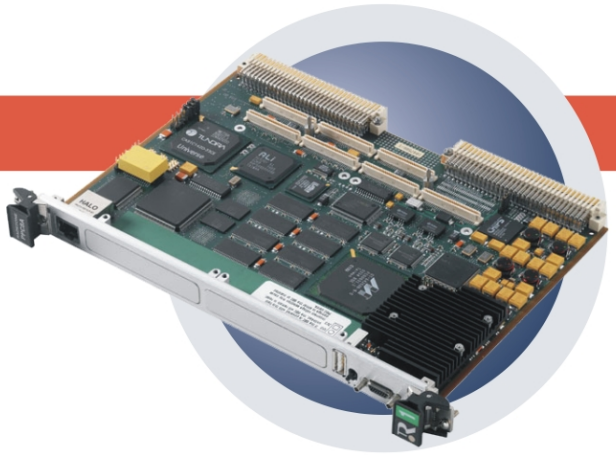
HARDWARE PRODUCT MANUAL



PowerX Product Manual

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5th	December 2005	PPC4A Rev 7 and up - Appendix A PPC4B - Appendix B PPC6 Rev 6 and 7 - Appendix C PPC7A - Appendix D PPC7D – Appendix E PPC8A – Appendix F
6th	October 2006	PPC6 – Appendix sent to archive PPC4A – Appendix A updated to include rev 12 boards PPC4B - Appendix B PPC7A – Appendix C PPC7D – Appendix D Corrected PPC8A – Appendix E updated to include rev 3 & rev 4 boards
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1. Introduction

PowerX Family Overview

PowerX is a range of Single Board Computers (SBCs) that benefit from the significant engineering investment made by Radstone in the PowerPC processor family since 1994. All PowerX boards are fully hardware and software compatible, maintaining standard, open market interfaces allowing customers to protect their application investments through a clearly defined Technology Insertion strategy. PowerX covers a broad range of environmental requirements from industrial to fully rugged through 2 distinct product streams:

PowerXpress

PowerXpress is a range of SBCs specifically designed to meet the needs of systems in the sheltered defense environments typically found in naval, ground based and vetronics applications. Available in 2 air cooled ruggedization levels, the PowerXpress range offers real cost benefits resulting from its sharp focus on the sheltered COTS market, without sacrificing performance. PowerXpress offers Radstone PowerPC pedigree plus performance plus affordability - an unrivalled combination. Full deployed test firmware, configuration control, and other software/services are available for critical program support.

PowerXtreme

PowerXtreme SBCs deliver the same exceptional performance as the PowerXpress range, but also offer rugged survivability. Designed explicitly for operation in harsh environments, PowerXtreme boards incorporate state of the art design and manufacturing techniques to guarantee high performance in the most demanding of defense and aerospace applications. Available in 5 air and conduction cooled levels, with options for full deployed test firmware, configuration control and other services.

Build Styles

Like all Radstone's VME products, the PowerX family is available in a range of build styles, from Level 1 (Standard), suitable for a benign office-like environment, right through to Level 5 (Rugged Conduction-cooled), capable of withstanding the harshest of environments. All products are COTS/NDI, and make maximum use of low cost plastic packaged integrated circuits to ensure the most cost effective solution, whatever the market.

Add-on Functionality

PowerX boards have 2 on-board PMC sites, with PMC I/O available through the P0 and (optionally) P2 connectors, allowing direct backplane connection to all I/O. Further PMC sites are available using a P0CC1 companion carrier card.

Radstone is a key member of the VITA standards committee, setting the standards for rugged conduction-cooled PMCs.

A range of PMCs is available from Radstone in both conduction-cooled and air-cooled build standards. More details on these can be found at http://www.radstone.com, or product literature can be obtained from your nearest Sales Office or Radstone directly.

For use in chassis, Radstone offers backplane transition modules to convert the condensed P2 and P0 pinouts to industry-standard formats, plus 3U breakout panels offering a variety of industry standard connectors such as Serial I/O and 10/100BaseT. Internal cables and a basic set of external cables are available. These transition and I/O modules are intended for development use in a benign environment, and so are only available in level 1 or 2 build standards.

For more details see the I/O Modules Manual, publication number RT5154.

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Features

- PowerPC CPU and interface controller gives low power, low cost, high performance RISC CPU and system interfaces all on one device as main system resource
- On-board User SDRAM with optional ECC for memory intensive applications
- Five build level options, three air-cooled and two conduction-cooled, gives maximum component reuse across multiple platforms
- Two PCI expansion slots on-board give system expansion using IEEE P1386.1 standard single or double width PMCs
- Optional PCI expansion bridge (on a PMC card) and PMC carrier cards future proof your system design by enabling PCI sub-system expansion to add new, low cost interface capability as required
- Two serial COM ports plus optional asynchronous or synchronous serial channels, with protocol support for inter-system and/or legacy equipment connectivity
- On-board Ethernet controller giving 10/100BaseT or 10Base5
- Radstone COTS software support includes BIT, Boot firmware, BSPs and ESPs (with BCS) for LynxOS and VxWorks/Tornado
- Wide range of shrink-wrapped application software available
- User FLASH for execution of application code
- Real Time Clock (TOD/calendar)
- Two RS232 serial I/O channels up to 115.2 kbaud
- 64-bit VMEbus interface using the Tundra Universe II VMEbus interface chip. ANSI/VITA 1-1994 VME64 and VME64 extensions (5 row P1 and P2) compatible
- JTAG connections available
- High-resolution graphics (may use a PMC)
- Single slot 6U VME form factor for reduced system cost and slot count
- Range of 3U rear-mounting I/O modules
- CHRP (Map B)-based design
- Ultra-SCSI peripheral interface controller
- Direct connection for keyboard and mouse
- Floppy disk controller
- Parallel/printer port
- Optional software maintenance giving automatic software revision updates and technical support
- Optional hardware and on-board firmware configuration management service giving a unique part number requiring customer authorisation for changes in product revision status

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Software Support

Radstone's software strategy for PowerX allows fully integrated system-level solutions to be realised easily and with confidence. Off-the-shelf, layered software modules deliver the most from low-level hardware features while exploiting the best high-level debug and run-time functionality of popular COTS operating systems and communications modules.

The software products described below build on those available for previous generations of the PowerX family, so providing a common look, feel and interface for technology inserts.

Radstone has invested more than 50 man-years of engineering talent into the PowerPC architecture so that customers can develop market-leading products using the O/S and development environment best suited to their long term program requirements.

SilverChip Boot Firmware

Developed as an integral part of the Radstone PowerX strategy, the SilverChip Boot firmware provides a foundation layer to interface between the raw Radstone board hardware, with its highly programmable device set-ups and flexibility, and the supported Operating Systems, which require a straightforward booting and device interface model.

SilverChip includes comprehensive configuration facilities, interactive or auto-boot sequencing from a range of device types, automatic PCI resource allocation at initialisation, PCI display/interrogation utilities and other valuable features for system integrators.

SilverChip seamlessly absorbs memory or other speed and feature enhancements, giving the same look and feel to the O/S and the user application as the Radstone hardware models advance. This allows the constant use of latest technology in required areas without system impact. Where particular operating systems define the use of alternate boot methods (e.g. VxWorks bootroms), SilverChip technology is absorbed into such boot methodology.

Built In Test

PPC BIT probes from the lowest level of discrete on-board hardware up to Line Replaceable Unit level within a system, ensuring the highest degree of confidence in system integrity. BIT includes comprehensive configuration facilities, allowing automatic initialisation tests to be defined for the desired mix of system functionality and options. Further tests can be invoked interactively, giving BIT a valuable role as a field service tool. Both object and source code products are available.

Background Condition Screening

BCS supplements the BIT initialisation test coverage with further health screening that can co-exist with a standard COTS Operating System.

In contrast to a traditional BIT-style test, the intensity and coverage of which makes it destructive to operating systems, the configurable BCS package allows functions such as periodic checksumming, memory scrubbing, and others to be tailored for operation alongside the application in on-line conditions. Results are stored in FLASH in the same format as BIT results. Code is available for reading out BIT/BCS results under LynxOS and VxWorks.

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Operating System Support

In-house porting expertise for PowerPC based boards is focused on key operating systems, including Wind River Systems' VxWorks/Tornado and LynuxWorks' LynxOS. Other operating system ports, drivers for third party hardware and layered products are provided through strategic partnerships with dedicated third party vendors, able to offer high quality products and services complementary to the Radstone range. In this way, state of the art development environments and debug tools that are part of the above software products are made available for use on Radstone's flexible hardware architectures.

Please contact Radstone for availability of other operating systems in addition to the standard VxWorks and LynxOS offerings.

VxWorks/Tornado

Wind River System's VxWorks/Tornado distributed real-time operating system includes integrated networking facilities and a complete software development environment for UNIX hosts. It features a fast, multitasking kernel with pre-emptive scheduling, inter-task communications, multiprocessor support, symbolic and source-level debugging, performance monitoring and an I/O file system.

The full range of facilities are supported by BSPs for all Radstone CPU types, which have been validated by both Radstone and Wind River for the greatest confidence and ease of use. To complement the BSPs, many of Radstone's I/O and graphics products are also supported by libraries and drivers.

LynxOS

Created by LynuxWorks, LynxOS is compatible with UNIX V.3. It is POSIX compliant and supports X.11 (X-Windows), Motif, NFS and TCP/IP. Unlike conventional UNIX, it is fully pre-emptive to ensure that application tasks can be rescheduled if a higher priority task is ready.

BSPs and ESPs

Board Support Packages provide 'standard' support for the above operating systems, as defined by the operating system vendors. Radstone also provide Enhanced Support Packages for comprehensive hardware support in addition to that defined by the operating system vendors. This approach allows users to implement a verifiable BSP standard and yet not be locked out of using valuable extra features, which will adapt the BSP but shorten development times. ESP features may be added or removed as desired during development.

Typical features include VME DMA for VxWorks (not included in WindRiver's BSP definition) and VME enhancements like dynamic windowing and interrupt generation for LynxOS (not included in LynuxWorks' BSP definition. BCS is also part of the ESP.

Notes:

1) Although Radstone will make every effort to maintain functionality, due to the increasingly short lifetimes of system components, devices used to provide the I/O on the PowerX boards are not guaranteed to remain fixed in the future.
2) For this reason, hardware should be accessed only through mechanisms provided by the Operating System's "Hardware Independence" mechanism (BSP, residual data, etc.), and not directly by application software.
3) If a standard operating system is not being used, then it is recommended that applications are written in such a way as to minimise direct access to hardware resources, bearing in mind that changes may be necessary to support future iterations of the hardware.

Radstone supported Operating Systems guarantee compatibility at the application level through the Hardware Independence mechanisms mentioned above.

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About this Document

Objectives

- To guide the reader through configuration, installation and power-up of PowerX boards
- To provide the user with reference information on the specific PowerX boards (PPC4, PPC4A, PPC6 etc.)

Note: On-board firmware and other software (e.g. drivers, BSPs, ESPs etc.) are described in separate user guides.

Audience

This manual is written to cover, as far as possible, the range of people who will handle or use the PowerX board including (but not limited to):

- Inspectors
- Installation technicians
- Hardware and software engineers
- System managers

While every effort has been made to keep the description of configuration, installation and power-up as simple and user-friendly as possible, a certain amount of background knowledge on these subjects is assumed.

Scope

This manual describes:

- All build standards of the PowerX boards
- All variants of the PowerX boards

This manual mentions, but does not describe in detail:

- PMCs
- Carrier cards
- PowerX on-board firmware
- Other firmware such as drivers, BSPs, ESPs, etc.
- Application software

Structure

This manual is divided into 2 main parts: the first part contains all the information common to the PowerX family, and the second part (the appendices) contains the information specific to the family constituents (PPC4, PPC4A, PPC6 etc.)

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Conventions

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a 'D' subscript and binary numbers have a 'b' subscript. The prefix '0x' shows a hexadecimal number, following the 'C' programming language convention. Thus:

One dozen = 12_D = 0x0C = 1100_b

The multipliers 'k', 'M' and 'G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when 'K', 'M' and 'G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

Note: When describing transfer rates, 'k' 'M' and 'G' mean $*10^3$, $*10^6$ and $*10^9$ *not* $*2^{10}$, $*2^{20}$ and $*2^{30}$.

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and VMEbus terminology follows the more familiar convention that bit 0 is the LSB and bit n is the MSB.

Signal names ending with a tilde (~) denote active low signals; all other signals are active high.

This manual uses the following types of notice:

1) Notes call attention to important features or instructions, and are shown as follows:

Note: This is an example note entry.

2) Cautions call attention to actions that may cause system damage or loss of data, and are shown as follows:

CAUTION

This is an example caution entry.

3) Warnings call attention to actions that may cause risk of personal injury, and are shown as follows:

WARNING

This is an example warning entry.

4) Recommendations give guidance on procedures that may be tackled in a number of ways, and are shown as follows:

RECOMMENDATION

This is an example recommendation entry.

Hyperlinks are indicated by use of blue text. Links may be to other parts of the same document, other CD-ROM based manuals or web sites. The links may not operate correctly where this document is not accessed via the Radstone Manuals CD-ROM or Manuals web page.

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Safety Notices

Safety Summary

Observe the following general safety precautions during operation of this equipment. Failure to comply with these precautions or with specific Warnings and/or Cautions elsewhere in this manual violates safety standards of design, manufacture and intended use of the equipment. Radstone Limited trading as Radstone Technology assumes no liability for the user's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Radstone is aware. Take note of these warnings and take all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Equipment

To minimize shock hazard, connect the equipment chassis and rack/enclosure to an electrical ground. If AC power is supplied to the rack/enclosure, the power jack and mating plug of the power cable must meet International Electrotechnical Commission (IEC) safety standards.

Power Supplies

WARNINGS

Do not exceed the maximum rated input voltages or apply reversed bias to the assembly. If such conditions occur, toxic fumes may be produced due to the destruction of components. Power supply problems are to be dealt with only by qualified personnel

Backplane Requirements

CAUTION

Only use the PowerX boards in backplanes that supply power on both the J1 and J2 connectors

Flammability

All Radstone circuit boards are manufactured by UL- recognized/approved manufacturers and have a flammability rating of 94V-0.

EMI/EMC Regulatory Compliance

CAUTION

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used in a cabinet with adequate EMI protection

Radstone boards are designed using good EMC practises and, when used in a suitably EMC-compliant chassis, should maintain the compliance of the total system.

Radstone boards also comply with EN60950 (product safety), which is essentially the requirement for the Low Voltage Directive (73/23/EEC).

Air-cooled PowerX boards are designed for use in systems meeting VDE class B, EN and FCC regulations for EMC emissions and susceptibility.

Conduction-cooled PowerX boards are designed for integration into EMC hardened cabinets/boxes.

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Related Documents

Due to the complexity of some of the parts used on PowerX boards, it is not possible to include all the detailed data on all such devices in this document. The following is a list of the specifications and data sheets that provide any additional information required:

VME64 Specification ANSI/VITA 1-1994 April 1995. *VMEbus International Trade Association AZ 85253 USA.*

VME64 Extensions Specification. Not Yet Published. *VMEbus International Trade Association AZ 85253 USA.*

PCI Local Bus Specification, Revision 2.1, June 1 1995. *PCI Special Interest Group OR 98214 USA.*

PCI System Design Guide.

IEEE P1386 Draft Standard for a Common Mezzanine Card Family.

IEEE P1386.1 Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards.

IEEE Std 802.3 Local Area Networks: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) - (ETHERNET) (1985) *The Institute of Electronic and Electrical Engineers Inc., NY 10017 USA.*

ANSI X3.131-1986 - Small Computer System Interface (SCSI), *American National Standards Institute NY10036, USA.*

ANSI X3.131-1994 : Information Systems - Small Computer Systems Interface-2 (SCSI-2) *American National Standards Institute NY10036, USA.*

ANSI/EIA/TIA-232-E - Interface Between Data Terminal Equipment and Data Communications Equipment Employing Serial Binary Data Interchange (December 1991) *Electronic Industries Association, DC20006 USA.*

ANSI/EIA/TIA-422-B, Electrical Characteristics of Balanced Voltage Digital Interface Circuits (December 1978). *Electronic Industries Association, DC20006 USA.*

PowerPC Microprocessor Common Hardware Reference Platform: A System Architecture, Version 1.0 (November 1995). *Morgan Kaufmann publishers Inc. San Francisco, California USA.*

PowerPC Microprocessor Family: The Programming Environments, 1994. *IBM VT 05452-4299 or Motorola AZ 85036 USA.*

The PowerPC Architecture: A Specification for a New Family of RISC Processors, Second Edition. *Morgan Kaufmann publishers Inc. San Francisco, California USA.*

PowerPC 740/750 RISC Microprocessor User's Manual. *Motorola AZ 85036 USA.*

MPC7400 RISC Microprocessor User's Manual. Motorola *MPC7400UM/D.*

MPC106 PCI Bridge/Memory Controller User's Guide, 1/97. *Motorola AZ 85036 USA.*

MPC107 PCI Bridge/Memory Controller User's Guide. *Motorola AZ 85036 USA.*

NCR53C860 PCI-SCSI I/O Processor Data Manual. *NCR Microelectronic Products Division. CO 80916. USA.*

Digital Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller Hardware Reference Manual. *Advanced Micro Devices Inc. CA 94088-3453 USA.*

W83C553F System I/O Controller with PCI Arbiter Data Book. *Winbond Systems Laboratory.*

SMC37C93X Plug and Play Compatible Ultra I/O Controller. *Standard Microsystems Corporation.*

Universe II User Manual 1998. *Tundra Microsystems ON K2K 2M5 Canada.*

PowerSpanII User Manual. *Tundra Microsystems ON K2K 2M5 Canada.*

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FLASH Memory, Volume 1 1995. *Intel corporation IL 60056-7641 USA.*

Datacom ICs. 1991. *Zilog Inc. CA 95008-6600.*

Z8036 Z-CIO/Z8536 CIO Counter/timer and Parallel I/O Unit Technical Manual. *Zilog Inc. CA 95008-6600.*

Atmel Non-volatile Memory Data Book, 1995-1996, *Atmel, San Jose, CA 95131*

I/O Modules Manual, publication number RT5154.

SilverChip (PPC Boot Firmware) Manual, publication number RT5078.

PPCBoot Firmware User Manual, publication number PPCBOOT-0HL.

PowerX User Guide (BIT Edition), publication number PPCBIT-0HU.

PMCPCI Manual, publication number PMCPCI-0HH.

P0CC1 Manual, publication number P0CC1-0HH.

PMC Installation Note, publication number HN4/3-99.

PowerX User Guide (VxWorks Edition), publication number RT5138.

PowerX User Guide (Tornado/Platforms/VxWorks Edition), publication number PXBSP-PTR-0HU.

Note: Radsone Software/Firmware Release notes are also included with each release/update. These contain up-to-date information and must also be consulted.

World Wide Web Sites

Manufacturers of many of the devices used on the PowerX Boards maintain FTP or world-wide-web sites. Some useful sites for obtaining further relevant data are:

http://www.freescale.com	for Motorola PowerPC data
http://www-03.ibm.com/chips	for IBM PowerPC data
http://www.tundra.com	for PowerSpanII and Universe II chip information
http://www.vita.com	for VMEbus standards
http://www.ieee.com	for PCI Bus standards

Our world-wide-web is available at:

http://www.gefanucembedded.com/

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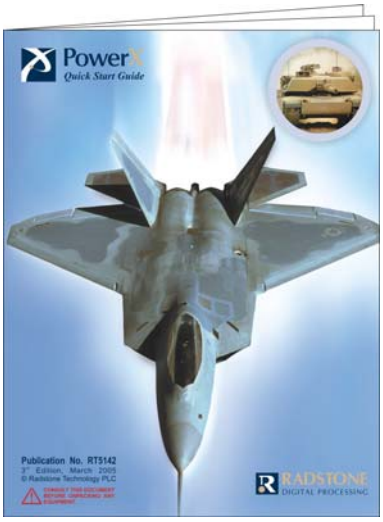
2. Getting Started

Initial Setup



For Initial unpacking, inspection, identification, configuration, installation, connection and startup instructions, refer to the Quick Start Guide supplied with the board. If, for any reason, a hardcopy of the Quick Start Guide is unavailable, clicking on the image opposite will open the copy stored on the CD-ROM/web site.

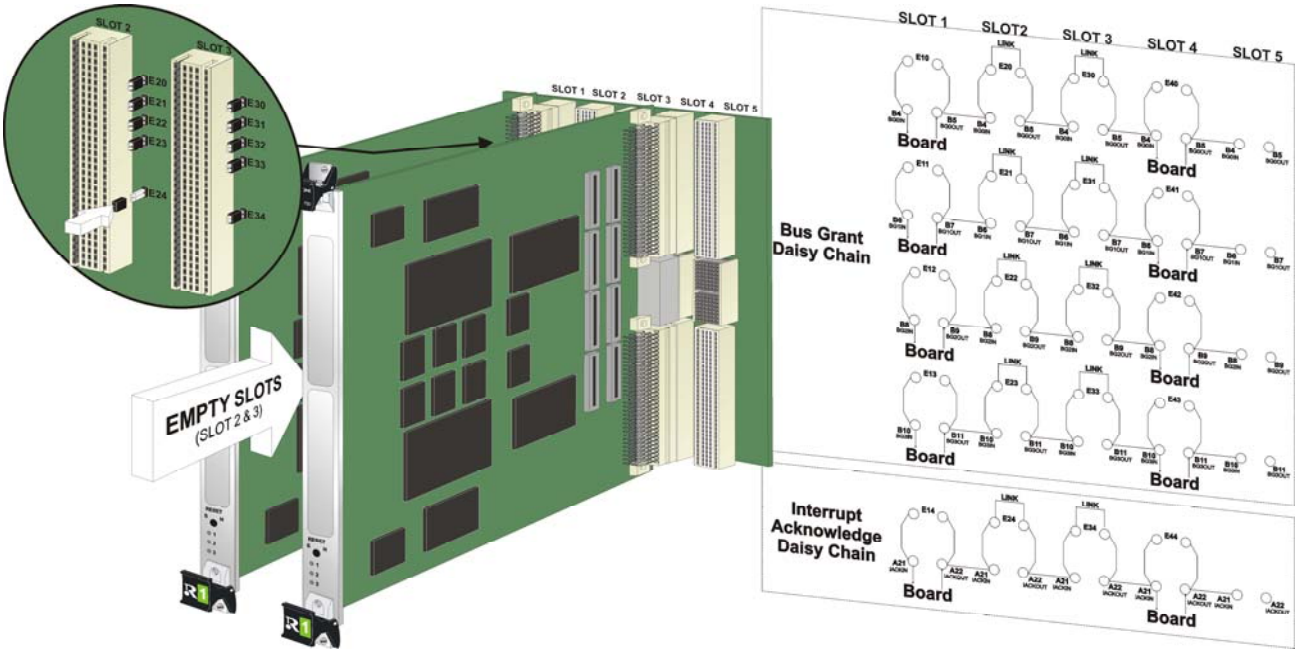
For more detailed hardware information, refer to the appropriate appendix.

Software documentation is available from the appropriate software platform vendor, and/or as Radstone documents included on this CD-ROM/web site.

To access any other CD-ROM/web based information, search using the menu system and/or search functions.

System Backplane Links

In order to use the PowerX board as a slave device, the rack's backplane configuration links must be correctly set. Radstone enclosures usually have two sets of links in the J1 (VMEbus) half of the backplane. The upper set of four links configures the Bus Grant (BGx) daisy chain and the lower link configures the Interrupt Acknowledge (IACK) daisy chain. They are provided so that the appropriate 'In' signal (BGxIN~/IACKIN~) at a particular slot can be connected to the corresponding 'Out' signal (BGxOUT~/IACKOUT~) at the same slot. This is only necessary when a slot position is not occupied by a board and there are boards further down the daisy chain – see the diagram below. Some backplanes have daisy chains that automatically link the signals across empty slots. See the manual appropriate to your enclosure for further details.



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3. Standard Interfaces

VME

VME is an open standard multi-processor bus with flexible address and data paths. It supports a maximum transfer rate of 40 Megabyte/sec (32bits), non-multiplexed and asynchronous data transfers, multi level interrupts and a maximum of 21 slots. The VMEbus standards are controlled and promoted by VITA (VME International Trade Association - http://www.vita.com/).

The VME interface standard is currently at Revision C (since 1985), with VME64 defined in 1994 (ANSI/VITA 1 – 1994) and VME64x following on in 1997 (ANSI/VITA 1.1 – 1997). For details of these standards, refer to the tables below.

The 4 main components of the VMEbus are:

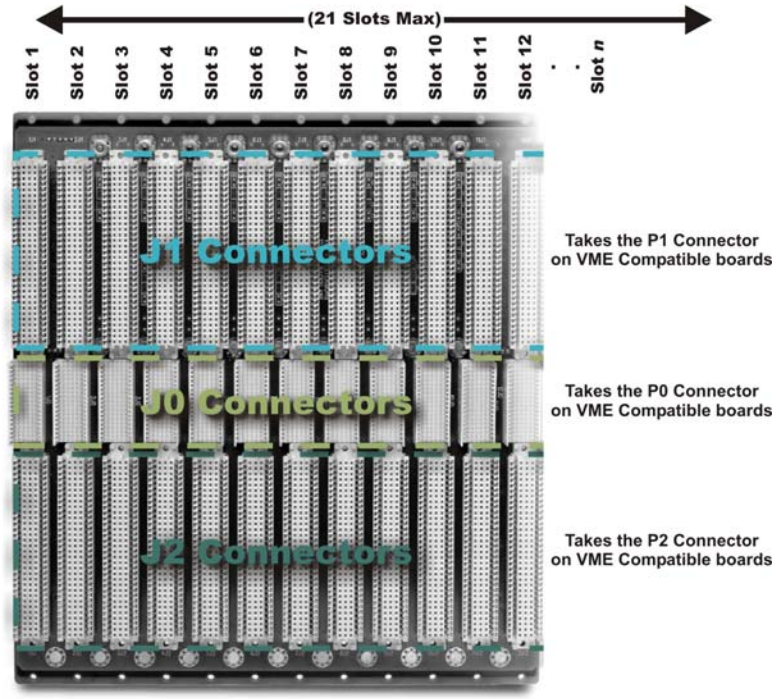
- Data Transfer Bus (16-bit, 32-bit or 64-bit)
- Arbitration Bus (4 levels)
- Interrupt Bus (7 Levels)
- Utility Bus

VME will support:

- 24-bit, 32-bit and 64-bit Addressing
- 8-bit, 16-bit & 32-bit Memory, I/O & Microprocessors
- An optional multi-purpose connector (J0)

These are dynamically defined on a cycle-by-cycle basis.

Figure 3.1 – VMEbackplane connector arrangement



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J1 Pin Assignment

Pin No.	Row z		Row a	Row b	Row c	Row d	
	VME64x	VME64	VME	VME	VME	VME64	VME64x
1	MPR	Reserved	D00	BBSY~	D08	Reserved	VPC
2	GND	GND	D01	BCLR~	D09	Reserved	GND
3	MCLK	Reserved	D02	ACFAIL~	D10	Reserved	+V1
4	GND	GND	D03	BG0IN~	D11	Reserved	+V2
5	MSD	Reserved	D04	BG0OUT~	D12	Reserved	RsvU-1
6	GND	GND	D05	BG1IN~	D13	Reserved	-V1
7	MMD	Reserved	D06	BG1OUT~	D14	Reserved	-V2
8	GND	GND	D07	BG2IN~	D15	Reserved	RsvU-2
9	MCTL	Reserved	GND	BG2OUT~	GND	Reserved	GAP~
10	GND	GND	SYSCLK	BG3IN~	SYSFAIL~	Reserved	GA0~
11	RTRY~	Reserved	GND	BG3OUT~	BERR~	Reserved	GA1~
12	GND	GND	DS1~	BR0~	SYSRESET~	Reserved	+3.3V
13	RsvBus1	Reserved	DS0~	BR1~	LWORD~	Reserved	GA2~
14	GND	GND	WRITE~	BR2~	AM5	Reserved	+3.3V
15	RsvBus2	Reserved	GND	BR3~	A23	Reserved	GA3~
16	GND	GND	DTACK~	AM0	A22	Reserved	+3.3V
17	RsvBus3	Reserved	GND	AM1	A21	Reserved	GA4~
18	GND	GND	AS~	AM2	A20	Reserved	+3.3V
19	RsvBus4	Reserved	GND	AM3	A19	Reserved	RsvBus5
20	GND	GND	IACK~	GND	A18	Reserved	+3.3V
21	RsvBus6	Reserved	IACKIN~	SERA	A17	Reserved	RsvBus7
22	GND	GND	IACKOUT~	SERB	A16	Reserved	+3.3V
23	RsvBus8	Reserved	AM4	GND	A15	Reserved	RsvBus9
24	GND	GND	A07	IRQ7~	A14	Reserved	+3.3V
25	RsvBus10	Reserved	A06	IRQ6~	A13	Reserved	RsvBus11
26	GND	GND	A05	IRQ5~	A12	Reserved	+3.3V
27	RsvBus12	Reserved	A04	IRQ4~	A11	Reserved	LI\I~
28	GND	GND	A03	IRQ3~	A10	Reserved	+3.3V
29	SBB	Reserved	A02	IRQ2~	A09	Reserved	LI\O~
30	GND	GND	A01	IRQ1~	A08	Reserved	+3.3V
31	SBA	Reserved	-12V	+5VSTDBY	+12V	Reserved	GND
32	GND	GND	+5V	+5V	+5V	Reserved	VPC

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J0 Pin Assignment

Pin No.	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
1	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
2	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
3	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
4	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
5	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
6	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
7	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
8	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
9	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
10	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
11	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
12	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
13	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
14	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
15	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
16	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
17	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
18	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
19	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND

Keying area on 80-way (Type A) connectors. The 95-way (Type B) connector is the preferred build option for most Radstone VME products.

Note: For actual PowerX board pin assignments, refer to the appropriate product Appendix.

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J2 Pin Assignment

Pin No.	Row Z		Row A	Row B	Row C	Row D	
	VME64x	VME64	VME	VME	VME	VME64	VME64x
1	User Defined	Reserved	User Defined	+5V	User Defined	Reserved	User Defined
2	GND	GND	User Defined	GND	User Defined	Reserved	User Defined
3	User Defined	Reserved	User Defined	RETRY~	User Defined	Reserved	User Defined
4	GND	GND	User Defined	A24	User Defined	Reserved	User Defined
5	User Defined	Reserved	User Defined	A25	User Defined	Reserved	User Defined
6	GND	GND	User Defined	A26	User Defined	Reserved	User Defined
7	User Defined	Reserved	User Defined	A27	User Defined	Reserved	User Defined
8	GND	GND	User Defined	A28	User Defined	Reserved	User Defined
9	User Defined	Reserved	User Defined	A29	User Defined	Reserved	User Defined
10	GND	GND	User Defined	A30	User Defined	Reserved	User Defined
11	User Defined	Reserved	User Defined	A31	User Defined	Reserved	User Defined
12	GND	GND	User Defined	GND	User Defined	Reserved	User Defined
13	User Defined	Reserved	User Defined	+5V	User Defined	Reserved	User Defined
14	GND	GND	User Defined	D16	User Defined	Reserved	User Defined
15	User Defined	Reserved	User Defined	D17	User Defined	Reserved	User Defined
16	GND	GND	User Defined	D18	User Defined	Reserved	User Defined
17	User Defined	Reserved	User Defined	D19	User Defined	Reserved	User Defined
18	GND	GND	User Defined	D20	User Defined	Reserved	User Defined
19	User Defined	Reserved	User Defined	D21	User Defined	Reserved	User Defined
20	GND	GND	User Defined	D22	User Defined	Reserved	User Defined
21	User Defined	Reserved	User Defined	D23	User Defined	Reserved	User Defined
22	GND	GND	User Defined	GND	User Defined	Reserved	User Defined
23	User Defined	Reserved	User Defined	D24	User Defined	Reserved	User Defined
24	GND	GND	User Defined	D25	User Defined	Reserved	User Defined
25	User Defined	Reserved	User Defined	D26	User Defined	Reserved	User Defined
26	GND	GND	User Defined	D27	User Defined	Reserved	User Defined
27	User Defined	Reserved	User Defined	D28	User Defined	Reserved	User Defined
28	GND	GND	User Defined	D29	User Defined	Reserved	User Defined
29	User Defined	Reserved	User Defined	D30	User Defined	Reserved	User Defined
30	GND	GND	User Defined	D31	User Defined	Reserved	User Defined
31	User Defined	Reserved	User Defined	GND	User Defined	Reserved	GND
32	GND	GND	User Defined	+5V	User Defined	Reserved	VPC

Note: For actual PowerX board pin assignments, refer to the appropriate product Appendix.

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VMEbus Signal Descriptions

Mnemonic	Signal Description
A01 to A15	**Address Bus (bits 1 to 15).** Address lines that are used to broadcast a short address
A16 to A23	**Address Bus (bits 16 to 23).** Address lines that are used with A01 to A15 and LWORD~ to broadcast a standard address
A24 to A31	**Address Bus (bits 24 to 31).** Address lines that are used with A01 to A23 and LWORD~ to broadcast an extended or 64-bit address
ACFAIL~	**AC Failure.** This shows that the AC input to the power supply is no longer being provided or that the required AC input voltage levels are not being met
AM0 to AM5	**Address Modifier (bits 0 to 5).** These are used to broadcast information such as the address size, cycle type, master identification or any combination of these
AS~	**Address Strobe.** This shows when a valid address has been placed on the address bus
BBSY~	**Bus Busy.** This is driven low by the requester associated with the current bus master to show that the master is using the bus
BCLR~	**Bus Clear.** This is generated by an arbiter to show that there is a higher priority request for the bus than the one being processed. This requests the current master to release the bus
BERR~	**Bus Error.** This is generated by a slave or bus timer to tell the master that the data transfer did not complete
BG0IN~ to BG3IN~	**Bus Grant (0 to 3) In.** These signals are generated by the arbiter to tell the board receiving it that if it is requesting the bus on that level, then it has been granted use of the bus. Otherwise the board should pass the signal down the daisy chain. The BGxIN~/BGxOUT~ signals form the bus grant daisy chain, i.e. the BGxOUT~ of one board forms the BGxIN~ of the next board in the daisy chain
BG0OUT~ to BG3OUT~	**Bus Grant (0 to 3) Out.** These signals are generated by requesters to tell the next board in the daisy chain that if it is requesting the bus on that level, then it can use the bus. Otherwise the board should pass the signal down the daisy chain
BR0~ to BR3~	**Bus Request (0 to 3).** A low level, generated by a requester, on one of these lines, shows that some master needs to use the bus.
D00 to D31	**Data Bus.** These are used to transfer data between masters and slaves, and status/ID information from interrupters to interrupt handlers
DS0~, DS1~	**Data Strobe 0, 1.** These are used with LWORD~ and A01 to show how many byte locations are being accessed (1, 2, 3 or 4). Also, during a write cycle, the falling edge of the first data strobe shows that valid data is available on the bus. On a read cycle, the rising edge of the first data strobe shows data has been accepted from the data bus
DTACK~	**Data Transfer Acknowledge.** This signal is generated by a slave. The falling edge shows that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle. The rising edge shows that the slave has released the data bus at the end of a read cycle
GAP	The geographical address parity [GAP~] is tied high or floating, depending upon the parity of the geographical address lines [GA0~-GA4~]. It is an open collector signal, and was added to the 160-pin J1 connector in the VME64x specification.
GA0~ to GA4~	**Geographic Address**. These are used to set the slave VME address of the board. GA0~ to GA3~ may be set to zero by fitting links E1 to E4 respectively. When GA4~ is not connected, a pull-up resistor pulls the signal high.
GND	The DC voltage reference for the system
IACK~	**Interrupt Acknowledge**. This is used by the interrupt handler to acknowledge an interrupt request. It is routed to the IACKIN~ pin of slot 1, where it is monitored by the IACK daisy chain driver
IACKIN~	**Interrupt Acknowledge In.** This tells the board receiving it that that board can respond to the interrupt acknowledge cycle in process or pass it down the daisy chain. IACKIN~/IACKOUT~ form the interrupt acknowledge daisy chain
IACKOUT~	**Interrupt Acknowledge Out.** This is sent by a board to tell the next board in the daisy chain that it can respond to the interrupt acknowledge cycle in progress

(Continued overleaf)

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(VMEbus Signal Descriptions continued)

MNEMONIC	SIGNAL DESCRIPTION
IRQ1~ to 7~	**Interrupt Request (1 to 7).** These are driven low by interrupters to request an interrupt on the corresponding level
LI/I~ & LI/O~	The **live insertion input/output** (LI/I~ & LI/O) signals are used to carry hot swap (live insertion) control information. They are three state driven signals and were added to the 160-pin J1 connector in the VME64x specification.
LWORD~	**Longword.** This is used with DS0~, DS1~ and A01 to select which byte location(s) within the 4-byte group are accessed during the data transfer
MCLK, MCTL, MMD, MPR, MSD	These signals are part of the IEEE 1149.5 MTM bus. They are three-state driven signals, which were added to the 160-pin /J1 connector in the VME64x specification.
Reserved	This signal is reserved for future enhancements of the VME specification
RETRY~	RETRY~, together with BERR~, can be asserted by a slave to postpone a data transfer. The master must then attempt the cycle again at a later time. The retry cycle prevents deadlock (deadly embrace) conditions in bus-to-bus links and secondary buses. RETRY~ is a standard three-state signal. The RETRY~ signal was added in the ANSI/VITA 1-1994 VME64 version of the bus specification. This pin was RESERVED in earlier versions. However, boards that support RETRY~ should work just fine with older backplanes, as they were required to bus and terminate this signal line.
RsvBus1 to RsvBus12	The reserved/bused RsvBus signals should not be used. VME64x backplanes must bus and terminate theses signals. They were added to the 160-pin J1 connector in the VME64x specification.
RsvU-1 & RsvU-2	The reserved/unbused RsvU signals should not be used. VME64x backplanes must not bus or terminate these signals. They were added to the 160-pin J1 connector in the VME64x specification.
SERA	The serial clock used to synchronize the data transmission on the serial bus.
SERB	This is used for serial data transmission.
SYSCLK	**System Clock.** This provides a constant 16 MHz clock signal that is independent of any other bus timing.
SYSFAIL~	**System Fail.** Shows a failure has occurred in the system. This signal can be generated by any system board
SYSRESET~	**System Reset.** When this is low, it causes the system to be reset
User Defined	Defined by the inserted hardware, these P0/P2 pins are predominantly used to route I/O signals from the inserted VME board via pass-through pins to Backplane Transition Modules (paddle cards). See the appropriate Connector sections in Hardware Appendices for pin assignments and signal definitions.
VPC	Voltage pre-charge [VPC] pins forma a 'make first / break last' contact. They are intended to be used as pre-charge power sources for live insertion logic. These pins were added to the 160 pin J1 and J2 connectors in the VME64x specification. The VPC pins are connected to the +5 VDC power supply on VME64x backplanes. These pins may also be used as additional +5 VDC power pins in boards that do not support live insertion.
WRITE~	**Write.** This is generated by a master to show whether the data transfer cycle is a read or a write
+5VSTDBY	**+5 Volts DC Standby.** This supplies +5V DC to devices requiring battery back-up
+5V	+5 Volts DC power
+12V	+12 Volts DC power
-12V	-12 Volts DC power

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Geographical Address Pin Assignments (VME64x)

Slot Number	GAP* Pin J1-D9	GA4* Pin J1-D17	GA3* Pin J1-D15	GA2* Pin J1-D13	GA1* Pin J1-D11	GA0* Pin J1-D10
1	Open	Open	Open	Open	Open	GND
2	Open	Open	Open	Open	GND	Open
3	GND	Open	Open	Open	GND	GND
4	Open	Open	Open	GND	Open	Open
5	GND	Open	Open	GND	Open	GND
6	GND	Open	Open	GND	GND	Open
7	Open	Open	Open	GND	GND	GND
8	Open	Open	GND	Open	Open	Open
9	GND	Open	GND	Open	Open	GND
10	GND	Open	GND	Open	GND	Open
11	Open	Open	GND	Open	GND	GND
12	GND	Open	GND	GND	Open	Open
13	Open	Open	GND	GND	Open	GND
14	Open	Open	GND	GND	GND	Open
15	GND	Open	GND	GND	GND	GND
16	Open	GND	Open	Open	Open	Open
17	GND	GND	Open	Open	Open	GND
18	GND	GND	Open	Open	GND	Open
19	Open	GND	Open	Open	GND	GND
20	GND	GND	Open	GND	Open	Open
21	Open	GND	Open	GND	Open	GND

Note: Geographical addressing is accessed/controlled via software (BSP), the function of which requires configuration before it may be used – see the appropriate BSP documentation.

For actual PowerX board pin assignments, refer to the appropriate product Appendix.

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PCI Bus

PCI provides a synchronous 32- or 64-bit multiplexed address and data bus at speeds of 33 or 66 MHz, allowing burst data transfers to 528 Mbytes/second. The PowerX architecture provides 2 PCI buses: one for internal PCI devices and one that allows communication with optional mezzanine expansion modules (PMCs). The internal PCI bus runs at 33 MHz and has a fixed data width of 32-bits. The PowerPC processor, Ethernet, Ultra-SCSI, VME interface controller and ISAbus Bridge (all of which have direct PCI connectivity) are attached to this bus, which provides a high-speed backbone for local interconnection of on-board devices. The Tundra Universe II chip provides full PCI to VME bridge capability.

As well as local interconnection of on-board devices, PCI also allows communication with optional mezzanine expansion modules (PMCs). The PCI mezzanine format also provides 64 I/O pins for user definition.

PCI Expansion

In addition to the 2 on-board slots supporting air- or conduction-cooled PMCs, the PowerX architecture offers expansion of slots via a family of standard PMC Carrier Cards.

The PCI sub-system can support from 2 to 9 PMCs in a standard VME chassis. The P0CC1 6U PMC Carrier is a single-slot replacement unit supporting 2 single-width or 1 double-width PMCs, which can be linked to the PowerX host via the P0/J0 interface on each card.

For those configurations requiring additional PCI functionality, Radstone's PCI Bridge PMC (PMCPCI) bridges the on-board PCI bus out via the P0 connector. Having done this, the user is free to:

- Use Radstone's range of P0 PMC carriers
- Interface PowerX boards directly to Radstone's range of SHARC-based DSP boards
- Multiprocess over PCI using Radstone's PPZero technology

In this way, PowerX boards can maintain concurrent bus operation, allowing applications using PMCs for routing and communications to operate efficiently and in parallel without being blocked.

See the P0BP1 Backplanes Product Manual, publication number P0BP1-0HH for more details.

PMC Sites

The PowerX family has two sets of connectors ({J11, J12, J14}, {J21, J22 and J24}) that allow two standard PMCs to be connected to the PCI bus.

The PMC I/O connectors are routed to the backplane connectors to allow backplane I/O on all styles. J14 (PMC site 1) is connected to P0 and, if fitted, J24 (PMC site 2) is connected to P2.

The PowerX fully supports front panel PMC I/O on build levels 1 to 3 and, with reduced functionality, on build levels 4 and 5.

While a level 4 or 5 PowerX board can only accept conduction-cooled PMCs, levels 1, 2 and 3 PowerX boards can accept either air-cooled or conduction-cooled PMCs, as long as adequate cooling is provided.

A range of air- and conduction-cooled PMCs is available from Radstone, all fully compliant with the appropriate standards. Air-cooled PMCs are defined in the IEEE 1386 Standard, and rugged conduction-cooled PMCs are defined in the ANSI/VITA 20-2001 Standard for Conduction-cooled PMCs.

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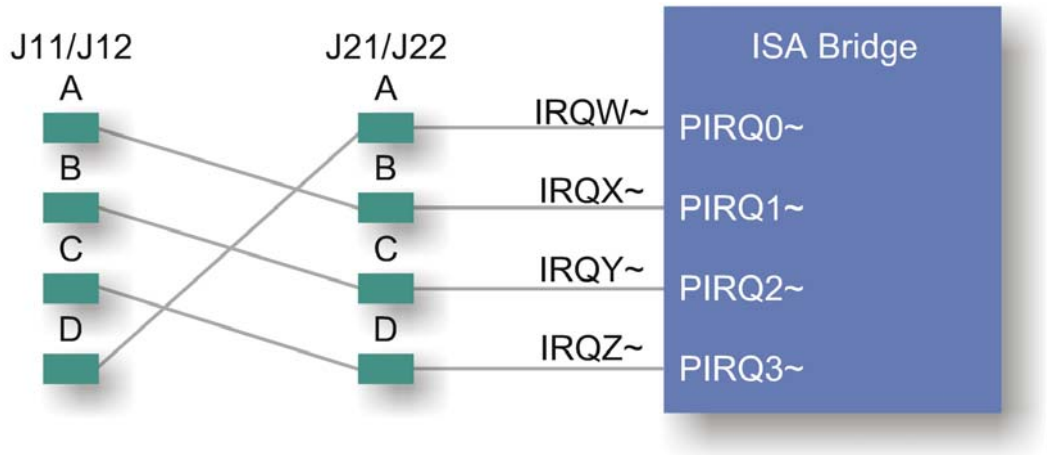
PCI Interrupts

There are 4 interrupt lines for the PMC slots on the PowerX board and the PMC carrier. These are connected to the PIRQ~ inputs of the interrupt controller. The PIRQ~ inputs may be routed to any IRQ that is set to level sensitive mode.

The interrupt routing follows the recommendations in the PCI specification and the PCI system design guide with a “rotation” between each slot.

The interrupt lines for the 2 PMC slots on the PowerX board are routed as shown below:



Two single function PMCs (which always use INTA~) are able to use unique IRQs with appropriate programming of the interrupt controller.

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PMC Interface

The IEEE P1386.1 standard defines four connectors with pin assignments shown in the following tables. Where 'J' is the host board connector ID (PMC mating connectors have a 'P' prefix), 'n' is the slot number (either 1 or 2), with the final number element defining the four possible connectors. For Host card layout information, see the layout diagram below.

Jn1, Jn2 & Jn3 Pin Assignments

Jn1/Pn1 32bit PCI			
Pin	Signal	Pin	Signal
1	TCK	2	-12V
3	GND	4	INTA~
5	INTB~	6	INTC~
7	BUSMODE1~	8	+5V
9	INTD~	10	PCI-RSVD
11	GND	12	3.3V aux
13	CLK	14	GND
15	GND	16	GNT~
17	REQ~	18	+5V
19	V (I/O)	20	AD[31]
21	AD[28]	22	AD[27]
23	AD[25]	24	GND
25	GND	26	C/BE[3]~
27	AD[22]	28	AD[21]
29	AD[19]	30	+5V
31	V (I/O)	32	AD[17]
33	FRAME~	34	GND
35	GND	36	IRDY~
37	DEVSEL~	38	+5V
39	GND	40	LOCK~
41	PCI-RSVD	42	PCI-RSVD
43	PAR	44	GND
45	V (I/O)	46	AD[15]
47	AD[12]	48	AD[11]
49	AD[09]	50	+5V
51	GND	52	C/BE[0]~
53	AD[06]	54	AD[05]
55	AD[04]	56	GND
57	V (I/O)	58	AD[03]
59	AD[02]	60	AD[01]
61	AD[00]	62	+5V
63	GND	64	REQ64~

Jn2/Pn2 32bit PCI			
Pin	Signal	Pin	Signal
1	+12V	2	TRST~
3	TMS	4	TDO
5	TDI	6	GND
7	GND	8	PCI-RSVD~
9	PCI-RSVD~	10	PCI-RSVD~
11	BUSMODE2~	12	+3.3V
13	RST~	14	BUSMODE3~
15	+3.3V	16	BUSMODE4~
17	PME~	18	GND
19	AD[30]	20	AD[29]
21	GND	22	AD[26]
23	AD[24]	24	+3.3V
25	IDSEL	26	AD[23]
27	+3.3V	28	AD[20]
29	AD[18]	30	GND
31	AD[16]	32	C/BE[2]~
33	GND	34	PMC-RSVD
35	TRDY~	36	+3.3V
37	GND	38	STOP~
39	PERR~	40	GND
41	+3.3V	42	SERR~
43	C/BE[1]~	44	GND
45	AD[14]	46	AD[13]
47	M66EN	48	AD[10]
49	AD[08]	50	+3.3V
51	AD[07]	52	PMC-RSVD
53	+3.3V	54	PMC-RSVD
55	PMC-RSVD	56	GND
57	PMC-RSVD	58	PMC-RSVD
59	GND	60	PMC-RSVD
61	ACK64~	62	+3.3V
63	GND	64	PMC-RSVD

Jn3/Pn3 64bit PCI			
Pin	Signal	Pin	Signal
1	PCI-RSVD	2	GND
3	GND	4	C/BE[7]~
5	C/BE[6]~	6	C/BE[5]~
7	C/BE[4]~	8	GND
9	V (I/O)	10	PAR64
11	AD[63]	12	AD[62]
13	AD[61]	14	GND
15	GND	16	AD[60]
17	AD[59]	18	AD[58]
19	AD[57]	20	GND
21	V (I/O)	22	AD[56]
23	AD[55]	24	AD[54]
25	AD[53]	26	GND
27	GND	28	AD[52]
29	AD[51]	30	AD[50]
31	AD[49]	32	GND
33	GND	34	AD[48]
35	AD[47]	36	AD[46]
37	AD[45]	38	GND
39	V (I/O)	40	AD[44]
41	AD[43]	42	AD[42]
43	AD[41]	44	GND
45	GND	46	AD[40]
47	AD[39]	48	AD[38]
49	AD[37]	50	GND
51	GND	52	AD[36]
53	AD[35]	54	AD[34]
55	AD[33]	56	GND
57	V (I/O)	58	AD[32]
59	PCI-RSVD	60	PCI-RSVD
61	PCI-RSVD	62	GND
63	GND	64	PCI-RSVD

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Jn4 Pin Assignments

The pin assignments marked User Defined I/O, are defined by PMC hardware and routed to the VME system backplane via the host system. For host card routing information, see the appropriate product appendix.

Pin	Signal	Pin	Signal
1	User Defined I/O	2	User Defined I/O
3	User Defined I/O	4	User Defined I/O
5	User Defined I/O	6	User Defined I/O
7	User Defined I/O	8	User Defined I/O
9	User Defined I/O	10	User Defined I/O
11	User Defined I/O	12	User Defined I/O
13	User Defined I/O	14	User Defined I/O
15	User Defined I/O	16	User Defined I/O
17	User Defined I/O	18	User Defined I/O
19	User Defined I/O	20	User Defined I/O
21	User Defined I/O	22	User Defined I/O
23	User Defined I/O	24	User Defined I/O
25	User Defined I/O	26	User Defined I/O
27	User Defined I/O	28	User Defined I/O
29	User Defined I/O	30	User Defined I/O
31	User Defined I/O	32	User Defined I/O
33	User Defined I/O	34	User Defined I/O
35	User Defined I/O	36	User Defined I/O
37	User Defined I/O	38	User Defined I/O
39	User Defined I/O	40	User Defined I/O
41	User Defined I/O	42	User Defined I/O
43	User Defined I/O	44	User Defined I/O
45	User Defined I/O	46	User Defined I/O
47	User Defined I/O	48	User Defined I/O
49	User Defined I/O	50	User Defined I/O
51	User Defined I/O	52	User Defined I/O
53	User Defined I/O	54	User Defined I/O
55	User Defined I/O	56	User Defined I/O
57	User Defined I/O	58	User Defined I/O
59	User Defined I/O	60	User Defined I/O
61	User Defined I/O	62	User Defined I/O
63	User Defined I/O	64	User Defined I/O

Note: For actual PowerX board pin assignments, refer to the appropriate product Appendix.

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PMC Signal Descriptions

Mnemonic	Description
AD[0] to AD[63]	**Address/Data bits.** Multiplexed address and data bus
C/BE[0]~ to C/BE[7]~	**Command/Byte Enables.** During the address phase, these signals specify the type of cycle to carry out on the PCI bus. During the data phase, the signals are byte enables that specify the active bytes on the bus
FRAME~	Driven low by the current master to signal the start and duration of an access
DEVSEL~	**Device Select.** Driven low by a PCI agent to signal that it has decoded its address as the target of the current access
PAR	**Parity.** Parity protection bit for AD0 to AD31 and BE0 to BE7
IRDY~	**Initiator Ready.** Driven low by the initiator to signal its ability to complete the current data phase
LOCK~	Driven low to indicate an atomic operation that may require multiple transactions to complete
BUSMODE2~	Driven low by a PMC module if it supports the current bus mode
BUSMODE2~ to BUSMODE4~	**Bus mode.** Driven by the host to indicate the bus mode
RST~	**Reset.** Driven low to reset the PCI bus
TRDY~	**Target Ready.** Driven low by the current target to signal its ability to complete the current data phase
PERR~	**Parity Error.** Driven low by a PCI agent to signal a parity error
SERR~	**System Error.** Driven low by a PCI agent to signal a system error
STOP~	Driven low by a PCI target to signal a disconnect or target-abort
INTA~	**Interrupt lines.** Level-sensitive, active-low interrupt requests
CLK	**Clock.** All PCI bus signals except RST~ are synchronous to this 33 MHz clock
REQ~	**Request.** Driven low by a PCI agent to request ownership of the PCI bus
GNT~	**Grant.** Driven low by the arbiter to grant PCI bus ownership to a PCI agent
IDSEL	**Initialisation Device Select.** Device chip select during configuration cycles
V (I/O)	+5V or +3.3V power to the PCI interface
PAR64	**Parity**. Parity protection bit for AD32 to AD63 and BE4 to BE7
REQ64~	**Request 64 Bit.** Driven low by PCI master to request 64 bit transfer
ACK64~	**Acknowledge 64 Bit.** Driven low by PCI agent in response to REQ64
M66EN~	Enable 66MHz operation
TCK	Test Clock. Clock for the PMC JTAG
TMS	Test Mode Select. Select Test Mode for PMC JTAG
TRST~	Test Reset. Reset any PMC JTAG devices
TDI	Test Data In. Input data for PMC JTAG chain
TDO	Test Data Out. Data from a PMC JTAG chain

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PMC Mapping to VME Backplane Connectors

The following tables show signal routing from the host PMC Jn4 connector to P0 and P2 backplane connectors as per ANSI/VITA 35 – 2000.

Mapping of PMC Jn4 to VME P0

PMC J4 Pin	VME P0 Pin	PMC J4 Pin	VME P0 Pin
1	4E	2	4D
3	4C	4	4B
5	4A	6	5E
7	5D	8	5C
9	5B	10	5A
11	6E	12	6D
13	6C	14	6B
15	6A	16	7E
17	7D	18	7C
19	7B	20	7A
21	8E	22	8D
23	8C	24	8B
25	8A	26	12E
27	12D	28	12C
29	12B	30	12A
31	13E	32	13D
33	13C	34	13B
35	13A	36	14E
37	14D	38	14C
39	14B	40	14A
41	15E	42	15D
43	15C	44	15B
45	15A	46	16E
47	16D	48	16C
49	16B	50	16A
51	17E	52	17D
53	17C	54	17B
55	17A	56	18E
57	18D	58	18C
59	18B	60	18A
61	19E	62	19D
63	19C	64	19B

Note: For actual PowerX board pin assignments, refer to the appropriate product Appendix.

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Single PMC Site Mapping of Jn4 to VME P2

PMC J4 Pin	VME P2 Pin Rows A & C	VME P2 Pin Rows D & Z	PMC J4 Pin	VME P2 Pin Rows A & C	VME P2 Pin Rows D & Z
1	1C	1D	2	1A	1Z
3	2C	2D	4	2A	3D
5	3C	3Z	6	3A	4D
7	4C	5D	8	4A	5Z
9	5C	6D	10	5A	7D
11	6C	7Z	12	6A	8D
13	7C	9D	14	7A	9Z
15	8C	10D	16	8A	11D
17	9C	11Z	18	9A	12D
19	10C	13D	20	10A	13Z
21	11C	14D	22	11A	15D
23	12C	15Z	24	12A	16D
25	13C	17D	26	13A	17Z
27	14C	18D	28	14A	19D
29	15C	19Z	30	15A	20D
31	16C	21D	32	16A	21Z
33	17C	22D	34	17A	23D
35	18C	23Z	36	18A	24D
37	19C	25D	38	19A	25Z
39	20C	26D	40	20A	27D
41	21C	27Z	42	21A	28D
43	22C	29D	44	22A	29Z
45	23C	30D	46	23A	31Z
47	24C		48	24A	
49	25C		50	25A	
51	26C		52	26A	
53	27C		54	27A	
55	28C		56	28A	
57	29C		58	29A	
59	30C		60	30A	
61	31C		62	31A	
63	32C		64	32A	

Note: For actual PowerX board pin assignments, refer to the appropriate product Appendix.

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Dual PMC Mapping of J14 & J24 to VME P2

PMC J14 Pin	VME P2 Pin	PMC J14 Pin	VME P2 Pin
1	17C	2	17A
3	18C	4	18A
5	19C	6	19A
7	20C	8	20A
9	21C	10	21A
11	22C	12	22A
13	23C	14	23A
15	24C	16	24A
17	25C	18	25A
19	26C	20	26A
21	27C	22	27A
23	28C	24	28A
25	29C	26	29A
27	30C	28	30A
29	31C	30	31A
31	32C	32	32A
33		34	
35		36	
37		38	
39		40	
41		42	
43		44	
45		46	
47		48	
49		50	
51		52	
53		54	
55		56	
57		58	
59		60	
61		62	
63		64	

PMC J24 Pin	VME P2 Pin	PMC J24 Pin	VME P2 Pin
1	1C	2	1A
3	2C	4	2A
5	3C	6	3A
7	4C	8	4A
9	5C	10	5A
11	6C	12	6A
13	7C	14	7A
15	8C	16	8A
17	9C	18	9A
19	10C	20	10A
21	11C	22	11A
23	12C	24	12A
25	13C	26	13A
27	14C	28	14A
29	15C	30	15A
31	16C	32	16A
33		34	
35		36	
37		38	
39		40	
41		42	
43		44	
45		46	
47		48	
49		50	
51		52	
53		54	
55		56	
57		58	
59		60	
61		62	
63		64	

Note: For actual PowerX board pin assignments, refer to the appropriate product Appendix.

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4. Build Styles and Dimensions

All Radstone's VME products are available in a range of build styles, from Level 1 (Standard), suitable for a benign office-like environment, right through to Level 5 (Rugged Conduction-cooled), capable of withstanding the harshest of environments. All products are COTS/NDI, and make maximum use of low cost plastic packaged integrated circuits to ensure the most cost effective solution, whatever the market.

There are two basic mechanical configurations: convection-cooled in accordance with ANSI/VITA 1-1994 specification and conduction-cooled in accordance with IEEE Std 1101.2-1992.

Convection-cooled boards include:

- Level 1
- Level 2
- Level 3

Conduction-cooled boards include:

- Level 4
- Level 5

A brief description of each build style follows:

Level 1

Intended for use in benign environments, Level 1 also provides the ideal cost effective method of complete system development. The Level 1 assembly comprises a double-Eurocard size printed wiring board with high quality commercial (plastic encapsulated) components. As software compatibility throughout the build styles is absolute, a system intended for final implementation in a severe tactical environment can be developed and debugged at low cost, switching over to target style only in the final stages of system integration.

Level 2

As Level 1, but conformally coated and 100% tested in manufacture to provide an extended operating range.

Level 3

Level 3 boards are intended for applications that have extended temperature, shock and vibration requirements, but can be served by conventional, forced-air-cooled, racking systems. These rugged boards comprise a double-Eurocard size printed wiring board fitted with wide temperature range, industrial grade components and are conformally coated as standard.

Level 4

Designed primarily for use in sealed ATR chassis and other conduction-cooled environments the Level 4 board features wide temperature range, industrial grade devices, an integral thermal management layer and incorporates a central stiffening bar for additional strength. Cooling is achieved through conduction of heat from the thermal management layer to the cold wall of the rack to which the boards are secured by screw driven wedgelocks. Level 4 boards are 100% temperature characterised and conformally coated during manufacture. Level 4 is mechanically compliant with IEEE Std. 1101.2-1992.

Level 5

As Level 4, but 100% tested in manufacture to provide an extended operating range.

All five styles fully support the power and versatility of the VMEbus, so no matter how large or diversified your project, absolute compatibility is assured at all stages of development.

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Environmental Specifications

	Build Style	Operating Temp (°C)	Storage Temp (°C)	Vibration	Shock	Humidity	Comments
Convection-cooled Boards	**Standard (Level 1)**	0 to +55 with airflow of 300 feet/minute	-50 to +100	0.002g^2/Hz from 10 to 2000 Hz random, and 2g sinusoidal from 5 to 500 Hz	20g peak sawtooth, 11ms duration	Up to 95% RH	Commercial grade cooled by forced air, for use in benign environments and software development applications.
	Extended Temp (Level 2)	-20 to +65 with airflow of 300 feet/minute	-50 to +100	0.002g^2/Hz from 10 to 2000 Hz random, and 2g sinusoidal from 5 to 500 Hz	20g peak sawtooth, 11ms duration	Up to 95% RH with varying temperature . 10 cycles, 240 hours	As Standard but conformally coated and temperature characterized.
	Rugged Air-cooled (Level 3)	-40 to +75 with airflow of 600 feet/minute	-50 to +100	0.04g^2/Hz from 10 to 2000 Hz with a flat response to 1000 Hz. 6db/Octave roll-off from 1000 to 2000 Hz	20g peak sawtooth, 11ms duration	Up to 95% RH with varying temperature . 10 cycles, 240 hours	Wide temperature rugged, cooled by forced air. Conformally coated for additional protection.
Conduction-cooled Boards	**Rugged Conduction-cooled (Level 4)**	-40 to +75 at the thermal interface	-50 to +100	Random 0.1g^2/Hz from 5 to 2000 Hz per MIL-STD-810E	40g peak sawtooth, 11ms duration	Up to 95% RH with varying temperature . 10 cycles, 240 hours	Mechanically compliant with IEEE 1101.2-1992. Designed for severe environment applications with high levels of shock and vibration, small space envelope and restricted cooling supplies. Conformally-coated as standard. Optional ESS.
	Rugged Conduction-cooled (Level 5)	-40 to +85 at the thermal interface	-50 to +100	Random 0.1g^2/Hz from 5 to 2000 Hz per MIL-STD-810E	40g peak sawtooth, 11ms duration	Up to 95% RH with varying temperature . 10 cycles, 240 hours	Mechanically compliant with IEEE 1101.2-1992. Designed for severe environment applications with high levels of shock and vibration, small space envelope and restricted cooling supplies. Conformally-coated as standard. Optional ESS.

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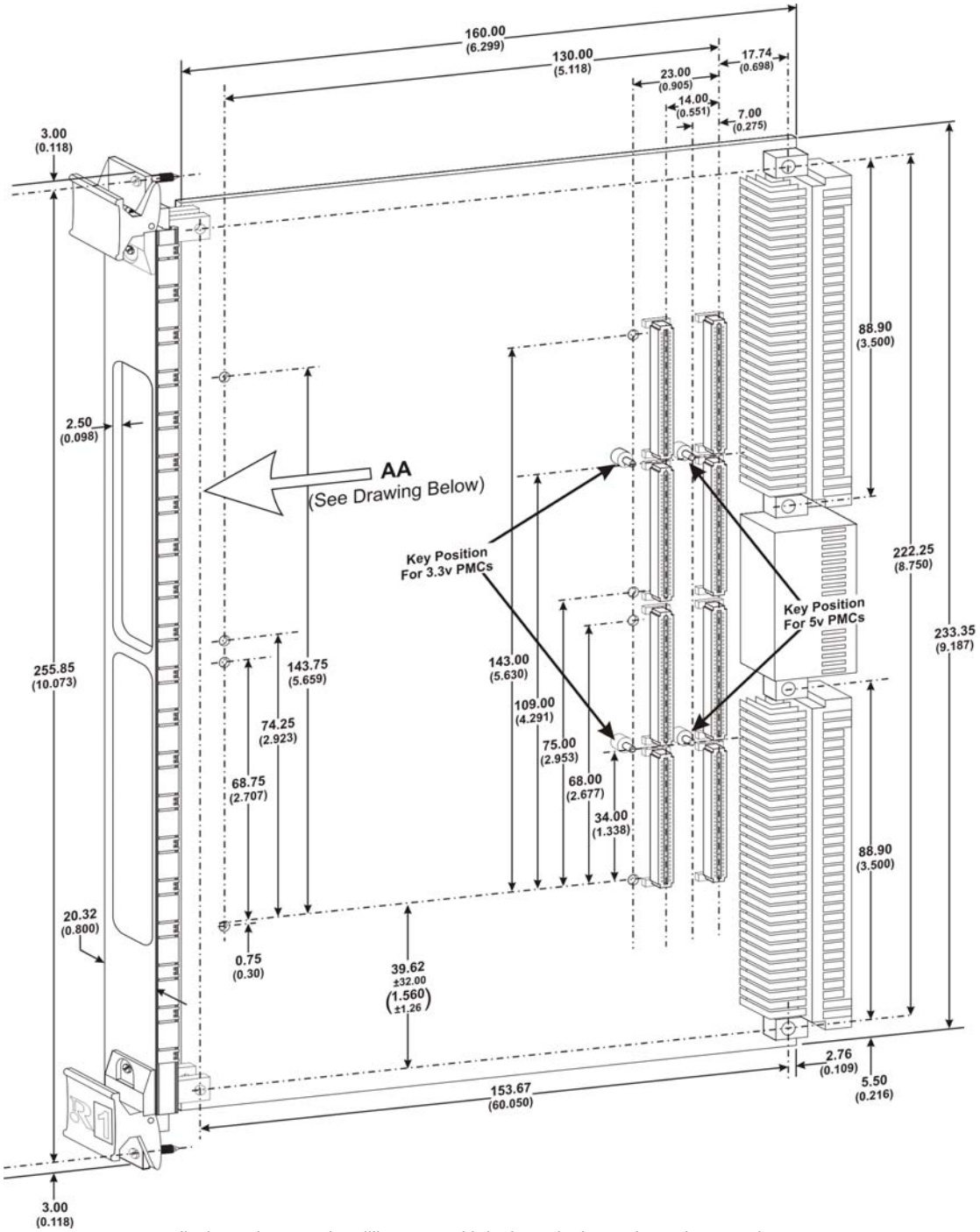
Mechanical Specifications

The following specifications are fully defined in ANSI/VITA and IEEE standards.

Convection Cooled Boards

The diagrams below show VME host board mechanical construction, as defined in ANSI/VITA 1 – 1994/1.1 – 1997 and IEEE 1386 - 2001/1386.1 - 2001.



All Dimensions are in millimeters, with inch equivalents shown in parentheses.

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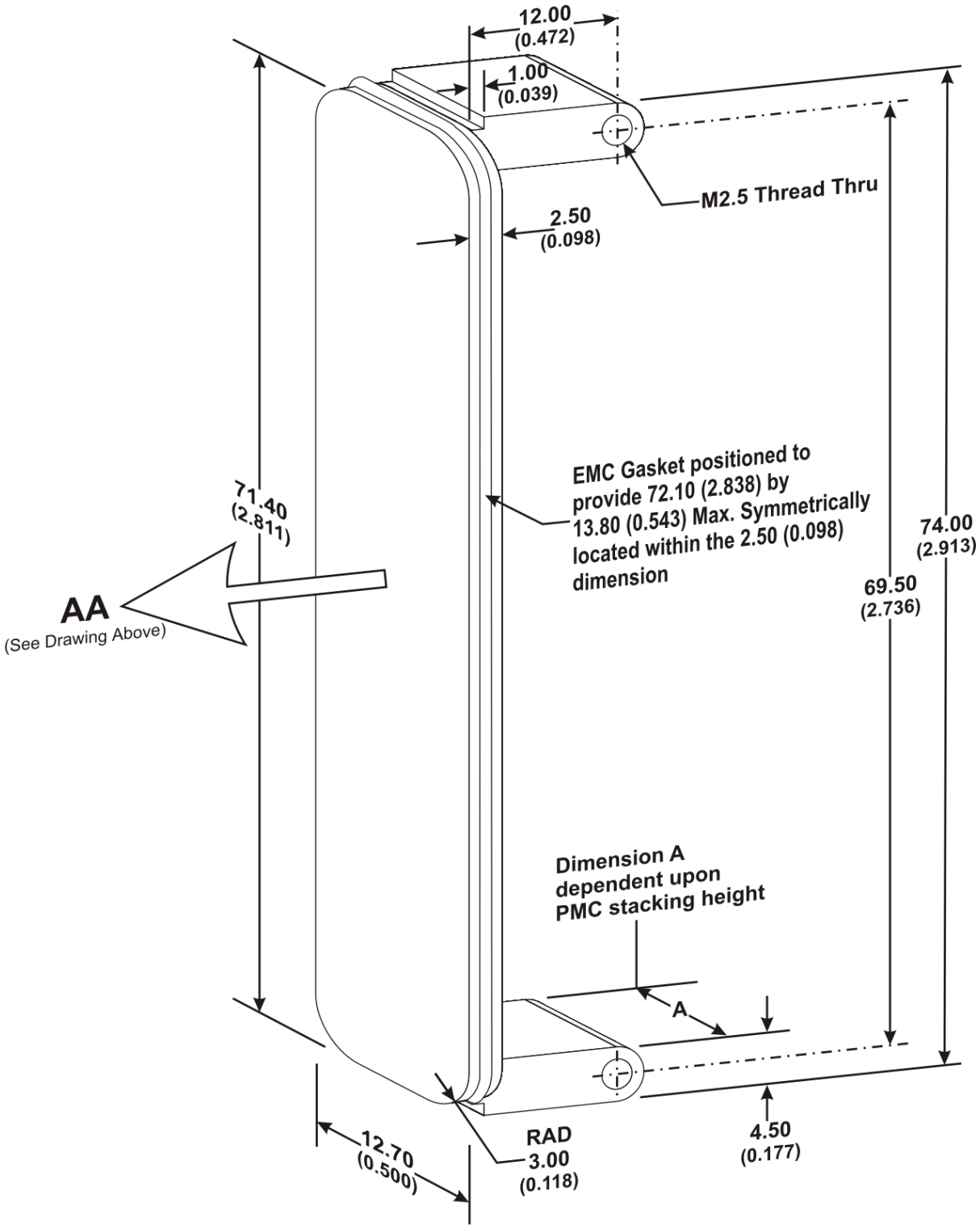
Note: Diagrams are included for guidance only. For full details, refer to the appropriate IEEE or ANSI/VITA documentation.



All Dimensions are in millimeters, with inch equivalents shown in parentheses.

Note: Diagrams are included for guidance only. For full details, refer to the appropriate IEEE or ANSI/VITA documentation.

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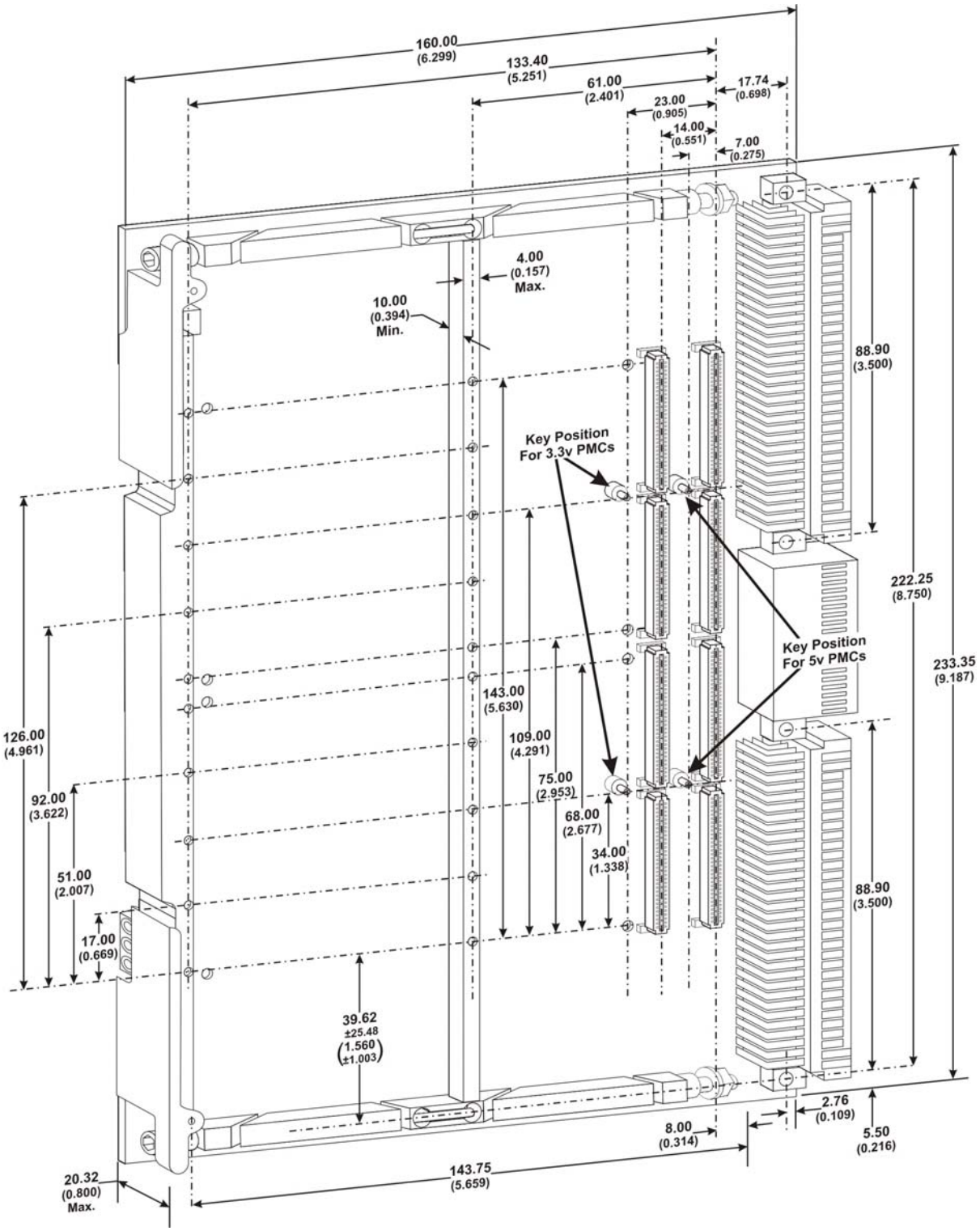
Conduction Cooled Boards

The diagram below shows VME host board mechanical construction, as defined in ANSI/VITA 1 – 1994, 1.1 – 1997 and 20 – 2001. Also IEEE 1101.2 - 1992, 1386 – 2001 and 1386.1 - 2001.



All Dimensions are in millimeters, with inch equivalents shown in parentheses.

Note: Diagrams are included for guidance only. For full details, refer to the appropriate IEEE or ANSI/VITA documentation.

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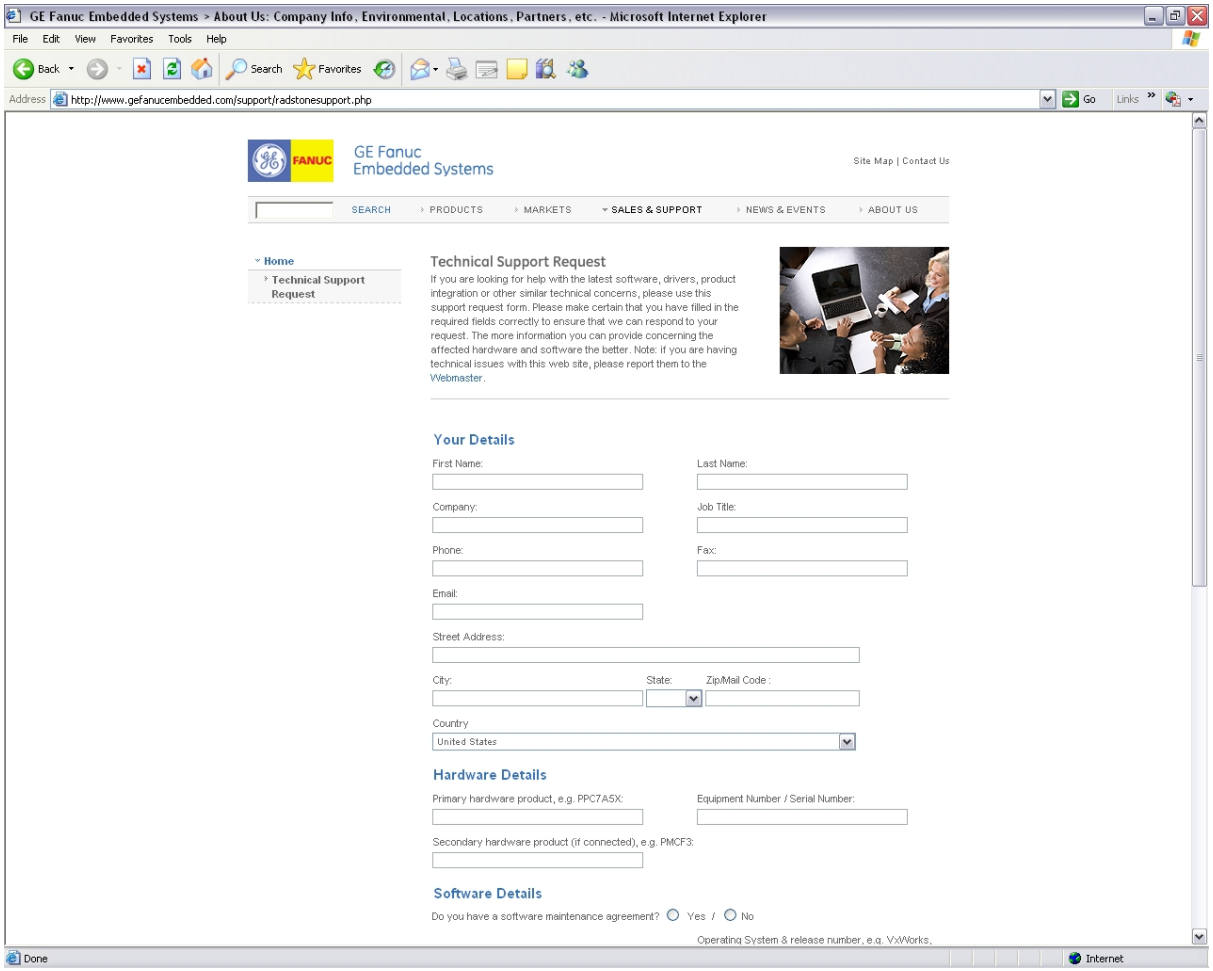
5. Technical Support

Radstone Contact Information

In the unlikely event that you experience problems with your PowerX board, for assistance please contact Radstone's Technical Help Line on:

+44 (0) 1327 322760

Alternatively, you may also register support requests using the Technical Support Request Form available through our web site at http://www.gefanucembedded.com/support/radstonesupport.php. This form looks like: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Last Name:
Company:
Job Title:
Phone:
Fax:
Email:
Street Address:
City:
State:
Zip/Mail Code :
Country
United States
Hardware Details
Primary hardware product, e.g. PPC7A5X:
Equipment Number / Serial Number:
Secondary hardware product (if connected), e.g. PMCF3:
Software Details
Do you have a software maintenance agreement? Yes / No
Operating System & release number, e.g. VxWorks,
Done
Internet

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6. Appendices

The following table includes hyperlinks to product specific appendices, together with links to their main sections. Each product appendix is stored as a separate Acrobat document.

Note: In common with all cross-document links, the hyperlinks will only operate when this document is viewed via Radstone's CD-ROM or website.

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Connectors	Connectors	Connectors	Connectors	Connectors	Connectors
Specifications	Specifications	Specifications	Specifications	Specifications	Specifications
Troubleshooting	Troubleshooting	Troubleshooting	Troubleshooting	Troubleshooting	Troubleshooting
Index	Index	Glossary	Glossary	Glossary	Glossary
		Index	Index	Index	Index

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